B. AMENDMENTS TO THE CLAIMS

Please amend the claims in accordance with the following complete listing of all claims in the application:

Claim 1 (currently amended): A programmable, single-chip embedded processor comprising:

(a) a multiple-bit, multithread processor core comprising a single processor pipeline ~~with four or more~~ having 'k' pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and the number 'n' of said processor threads being equal to or less than ~~the number of pipeline stages~~ "k";

(b) an instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set;

(c) a supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core, said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;

(d) a memory capable of storing data comprising instructions from said instruction set, said memory being internally integral to the processor, and comprising a main RAM and a boot ROM; and

(e) a peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core;

wherein:

~~(f) the processor core can concurrently execute as many as 'n' program threads in parallel, with each program thread moving serially through the pipeline;~~

~~and with each program thread being executed at a different pipeline stage at a given time; and~~

~~(g) the pipeline will complete one one-word instruction per clock cycle.~~

(f) each of the 'n' program threads occupies a unique pipeline stage at any given time;

(g) each program thread advances to the next pipeline stage with every clock cycle; and

(h) for a given program thread, the pipeline completes a one-word instruction every 'k' clock cycles.

Claim 2 (previously presented): An embedded processor as recited in Claim 1, wherein said processor pipeline includes an instruction fetch logic stage, an instruction decode logic stage, a multiple port register read stage, an address mode logic stage, an arithmetic logic unit for arithmetic and address calculations stage, a multiple port memory stage, a branch/wait logic stage, and a multiple port register write stage.

Claim 3 (previously presented): An embedded processor as recited in Claim 1, wherein said processor core supports one or more additional independent groups of at least two processor threads, each group of processor threads being associated with an instruction execution logic mechanism and a memory.

Claim 4 (previously presented): An embedded processor as recited in Claim 1, further comprising a condition code mechanism implemented in said instruction set for detecting specific word data types.

Claim 5 (previously presented): An embedded processor as recited in Claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range.

Claim 6 (previously presented): An embedded processor as recited in Claim 1, wherein said instruction set includes a processor instruction for enabling individual program threads to identify the particular processor threads on which they are being executed.

Claim 7 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is capable of examining, interpreting, and adjusting the state of the processor core for the purpose of starting and stopping individual processor threads, and modifying the state of each individual processor thread.

Claim 8 (previously presented): An embedded processor as recited in Claim 7, further comprising a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral adaptor and said memory.

Claim 9 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is capable of being accessed and controlled by one or more controlling threads selected from the processor threads in the processor core, by using input/output instructions to control the operation of one or more processor threads.

Claim 10 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are programmable.

Claim 11 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support MIMD operations.

Claim 12 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads can reconfigure the overall thread processing method of operation so that two or more processor threads can support SIMD operations.

Claim 13 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support simultaneously SIMD operations, and two or more processor threads can support MIMD operations.

Claim 14 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is operable by a first processor thread to start and stop the operation of another processor thread and to examine and alter processor core state information in single-step and multiple-step modes of controlled operation.

Claim 15 (previously presented): An embedded processor as recited in Claim 1, further comprising an identifying bit pattern embedded in said instruction set.

Claim 16 (previously presented): An embedded processor as recited in Claim 1, wherein said memory is expandable by addition of external memory accessible by the system through said peripheral adaptor.

Claim 17 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.

Claim 18 (previously presented): An embedded processor as recited in Claim 1, wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

Claim 19 (previously presented): An embedded processor as recited in Claim 15, wherein said identifying bit pattern is used to identify programming code for code protection purposes.

Claim 20 (previously presented): An embedded processor as recited in Claim 15, wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism.

Upon entry of the proposed amendments, the claims pending in the application will be **Claims 1-20.**